

FIG 1

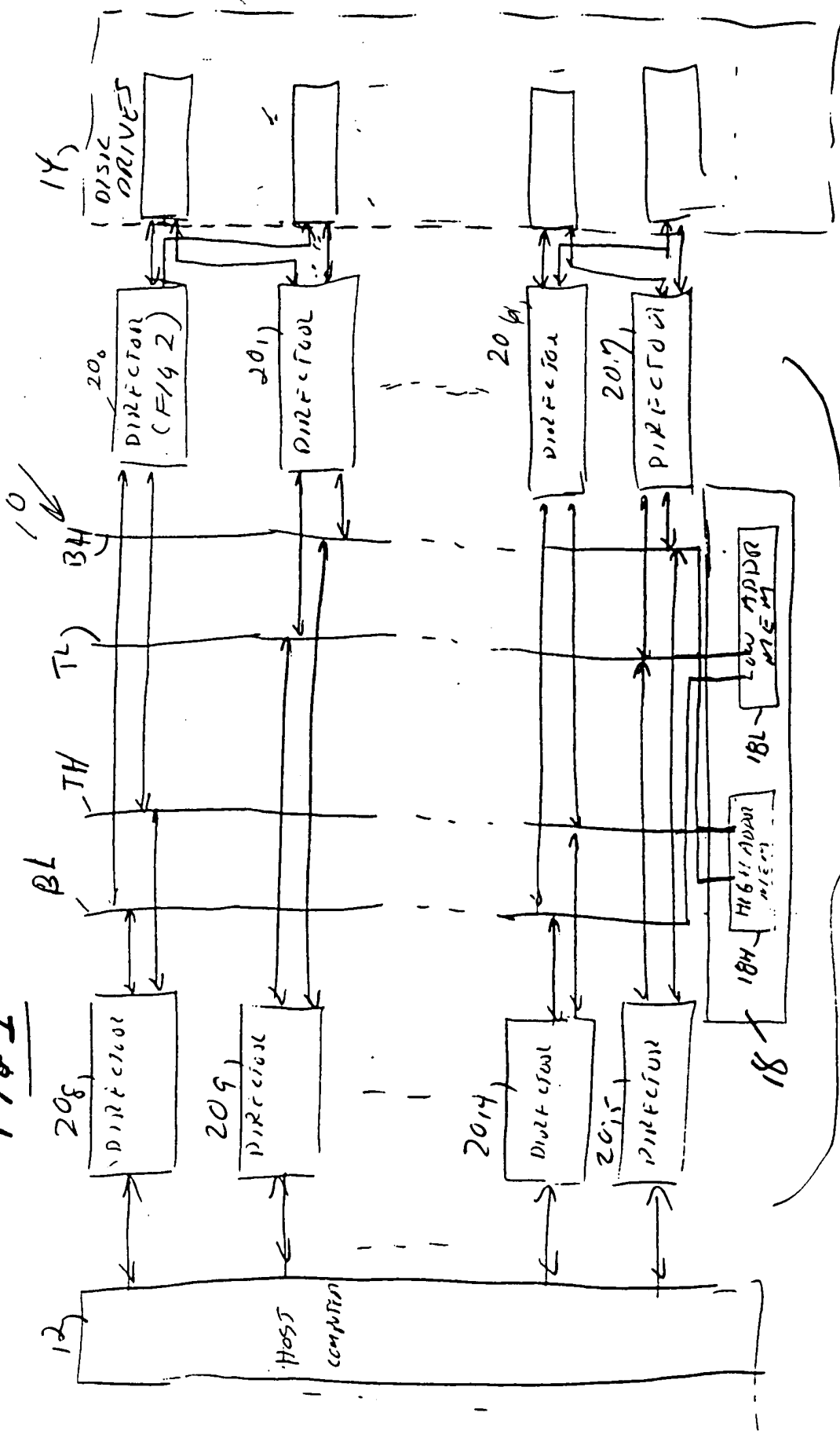
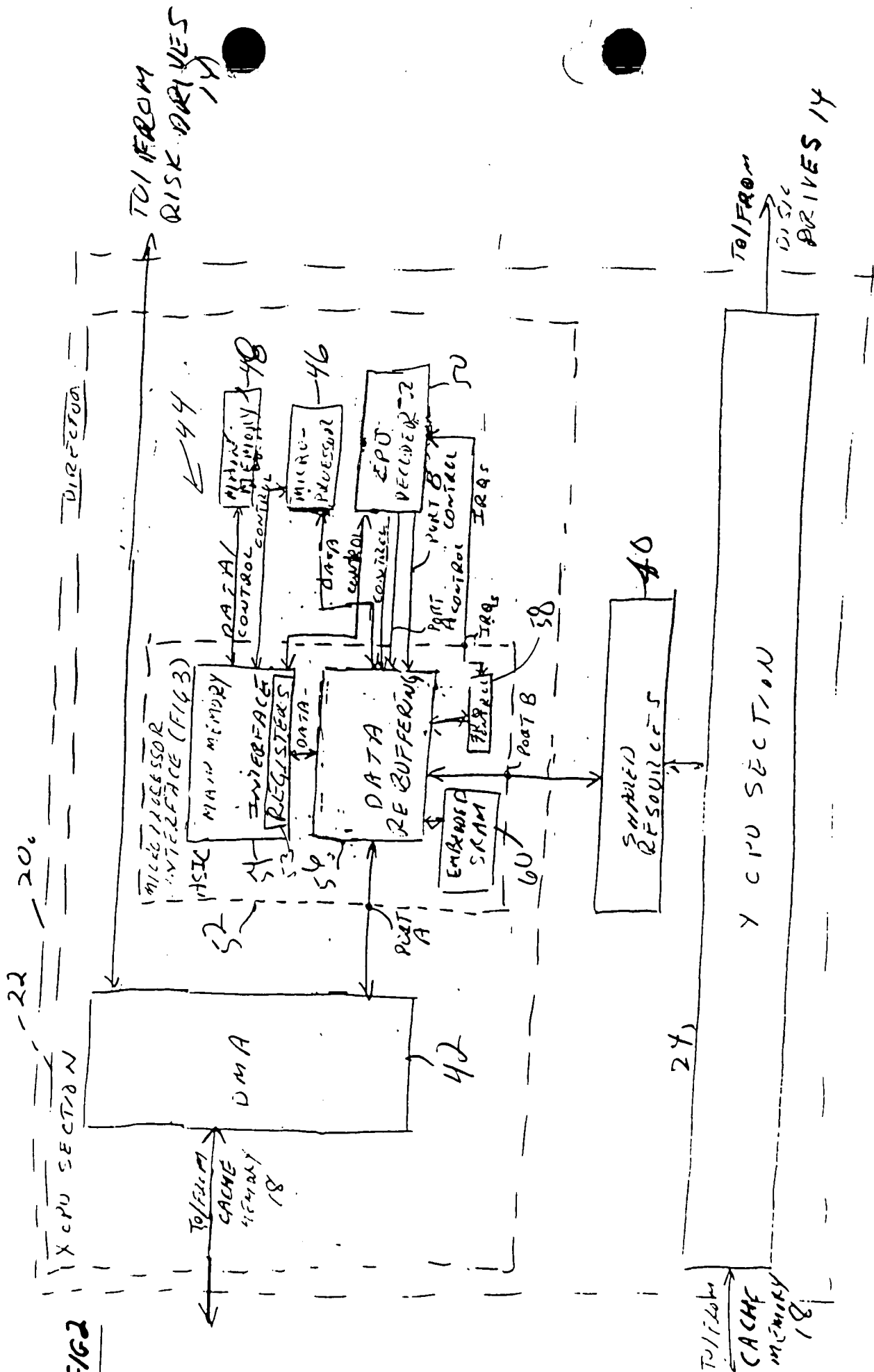


FIG 2



MICROCOLLE
INTERFACE

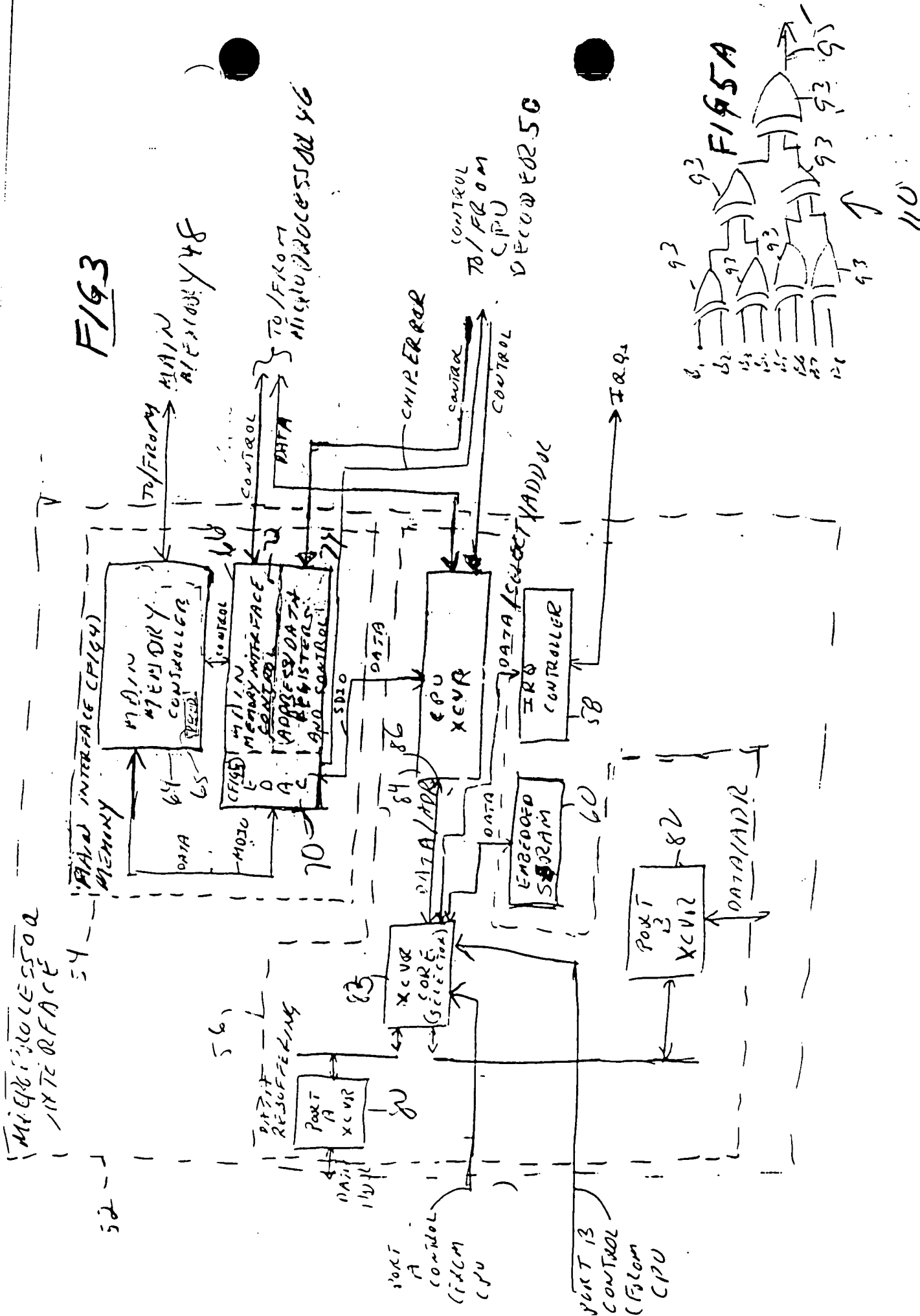
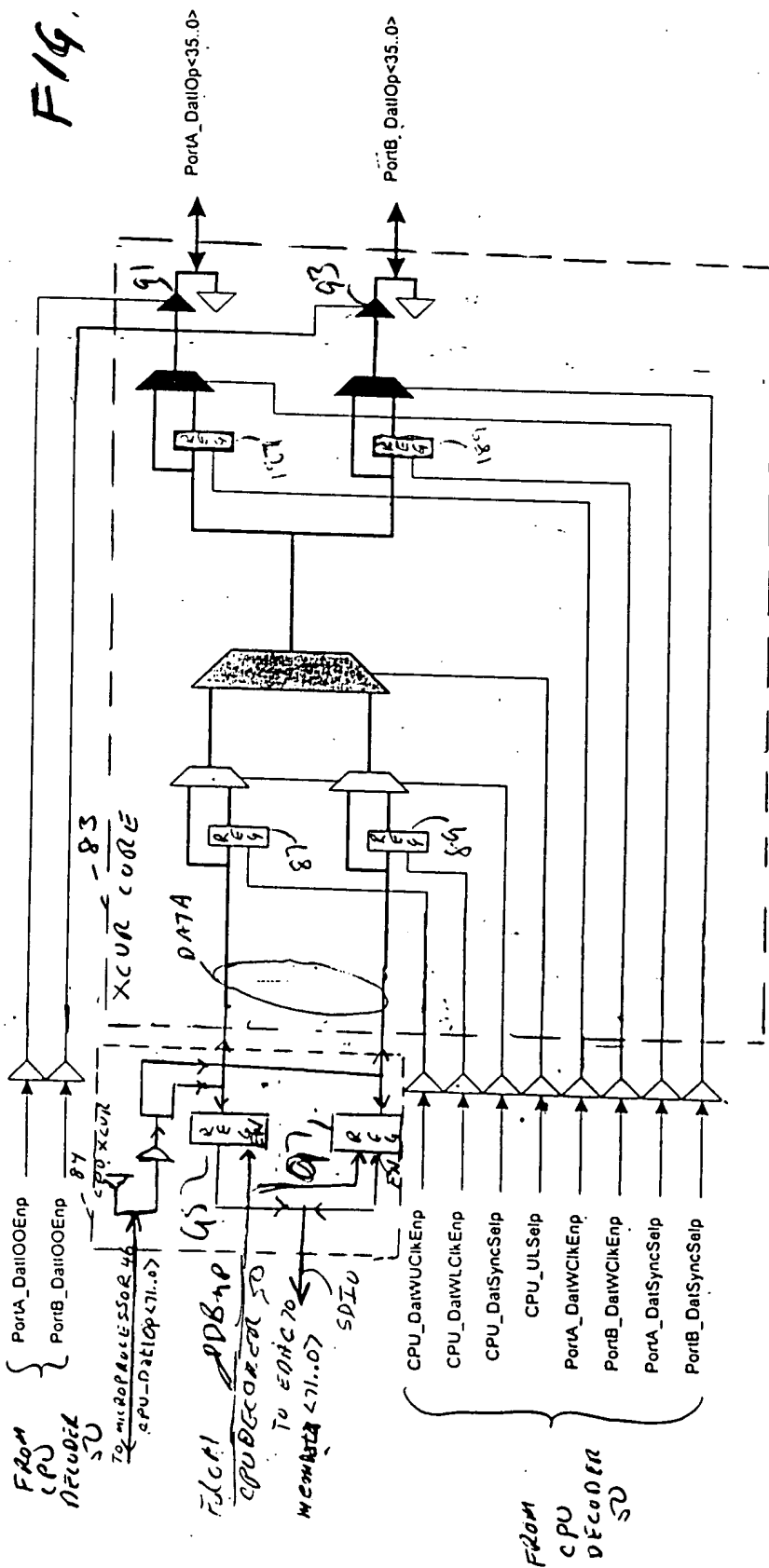


Fig. 3A



F/G3B

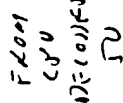
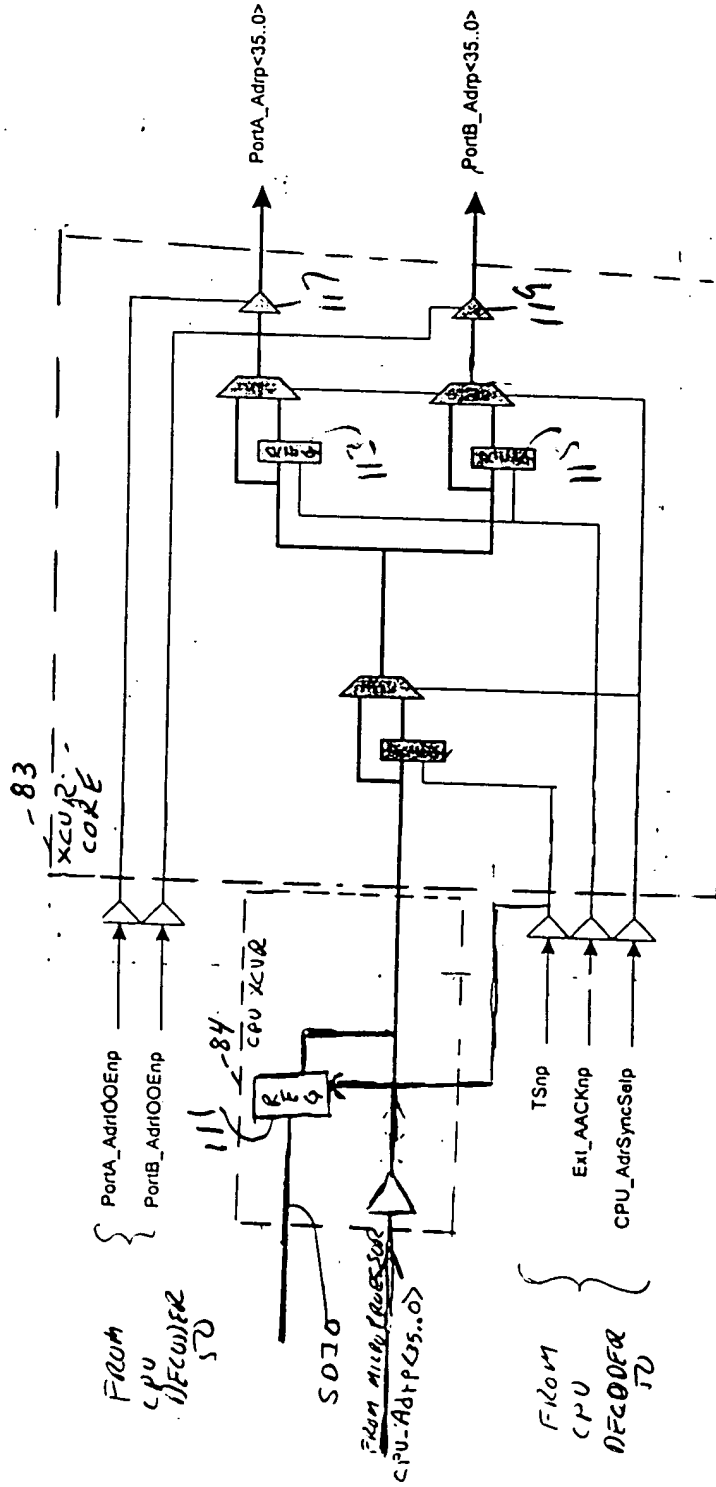


FIG 3C



F1G3D

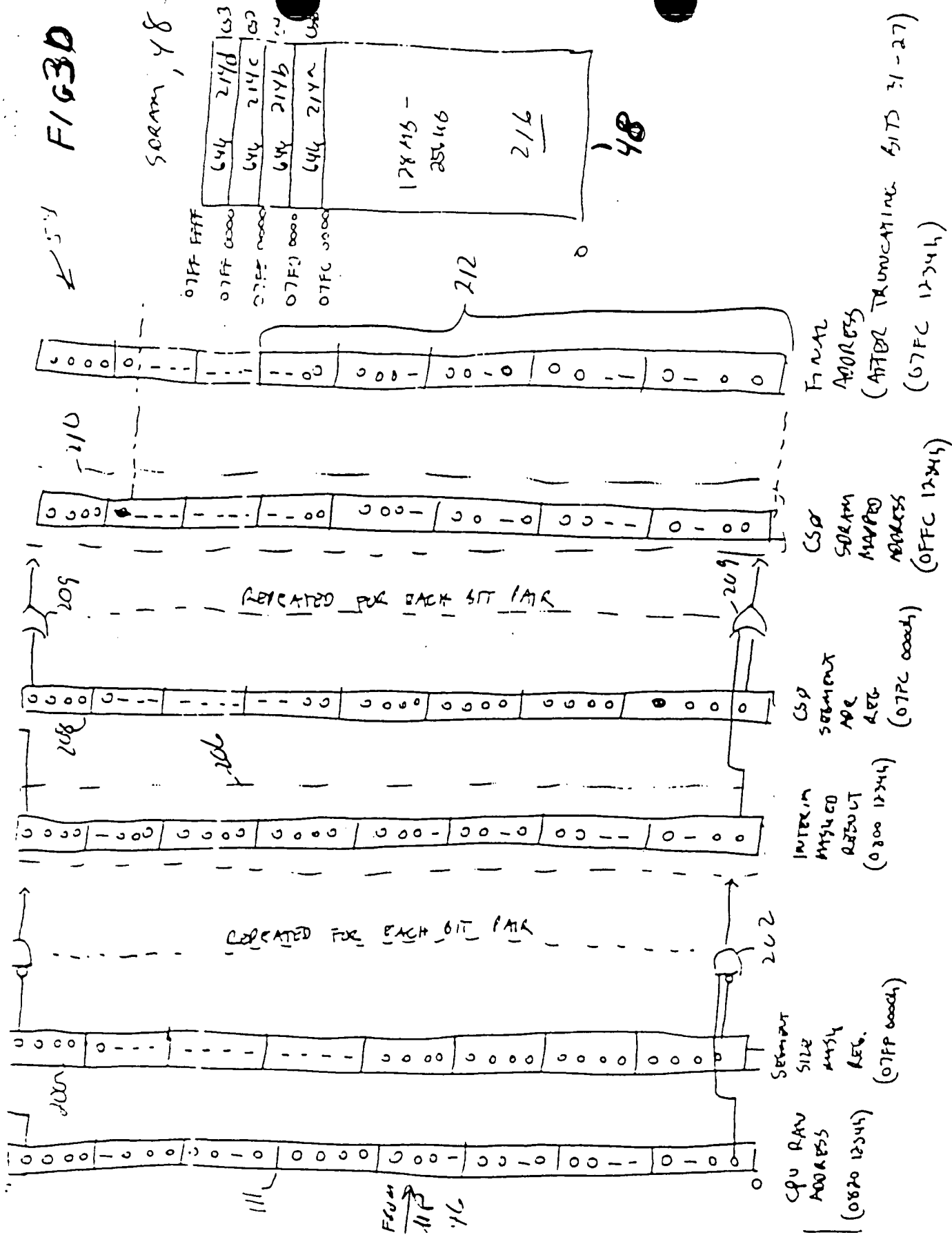


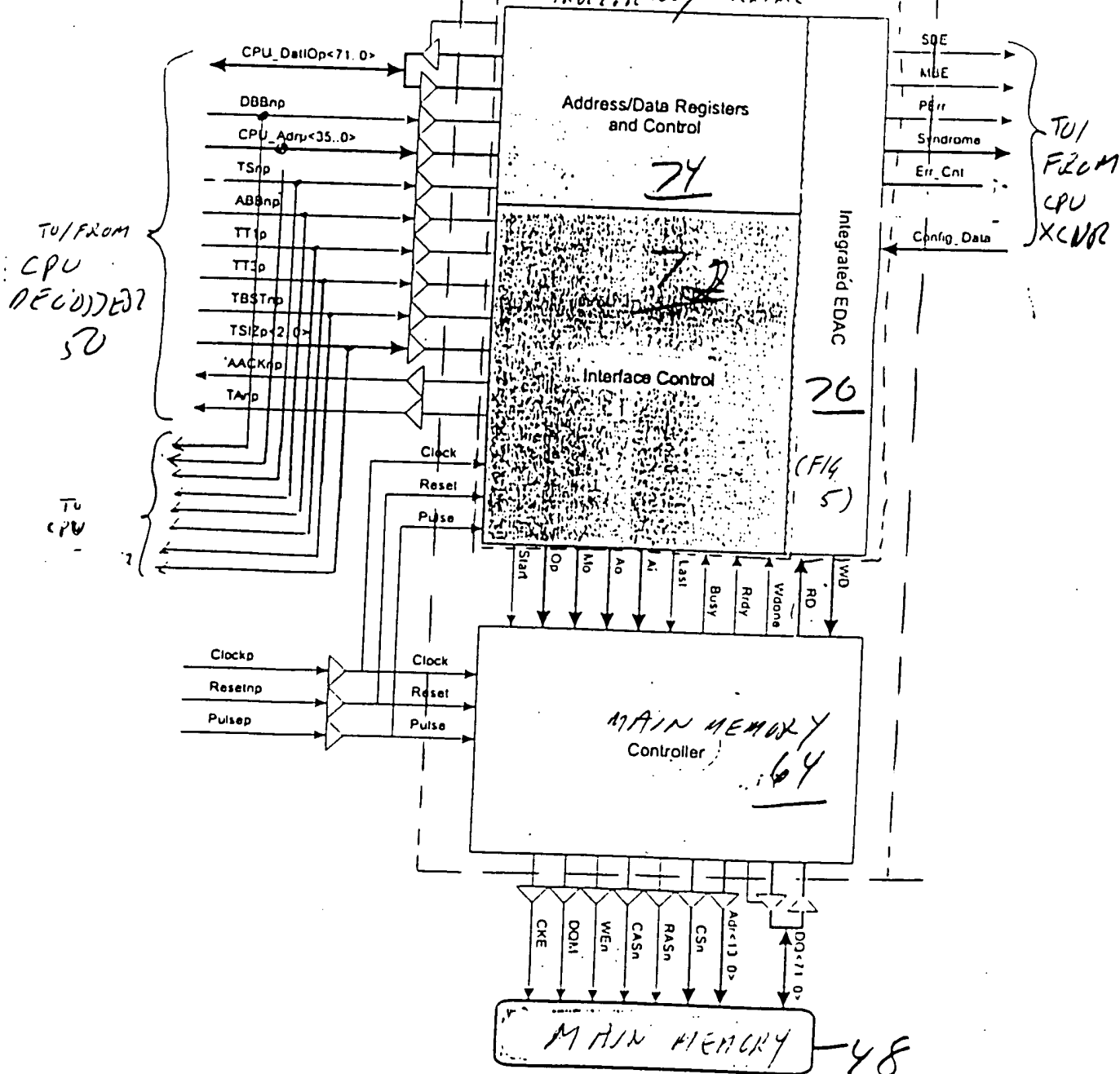
FIG 4

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MAIN MEMORY INTERFACE

MAIN MEMORY INTERFACE



INTERUPT CONTROLLER

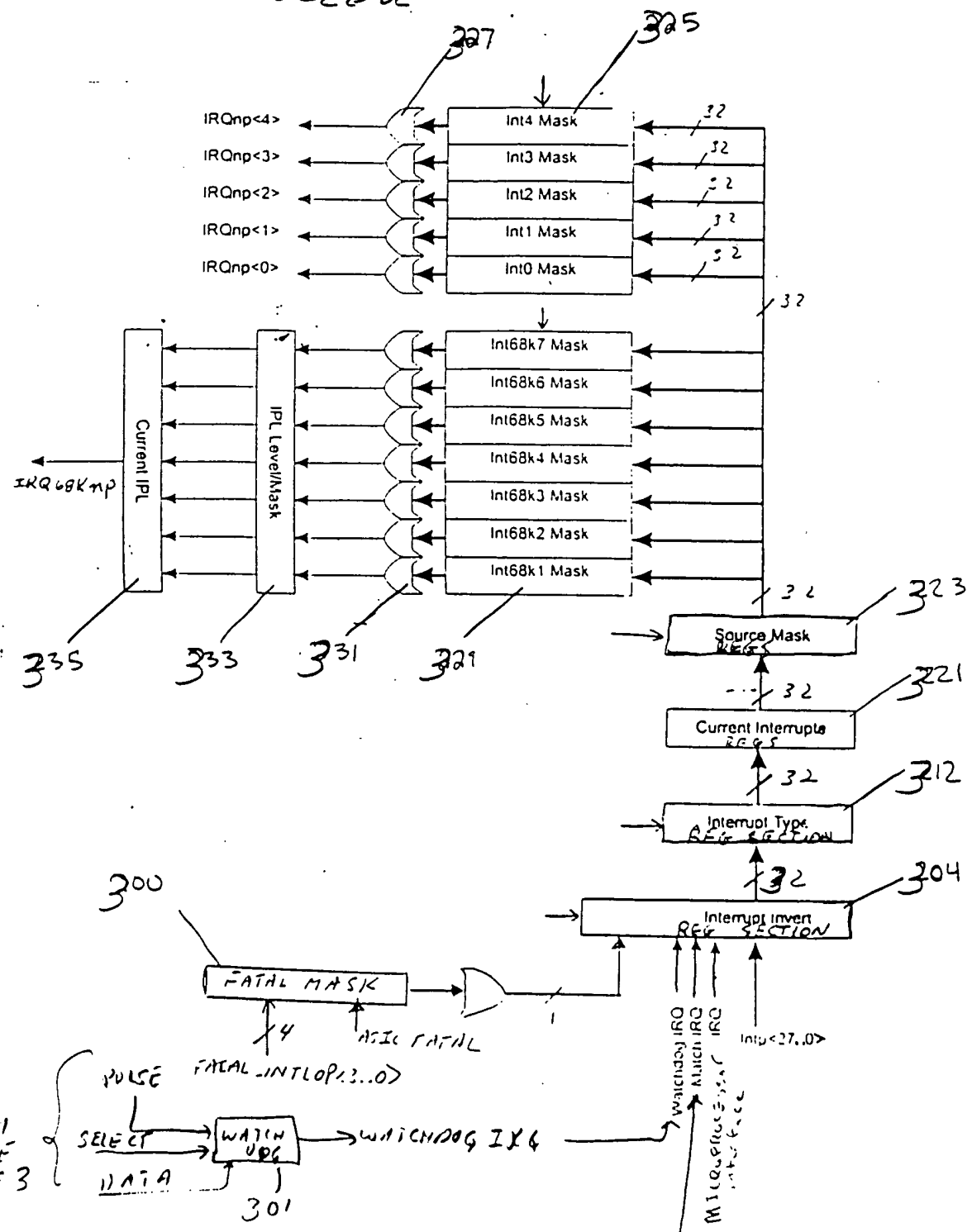
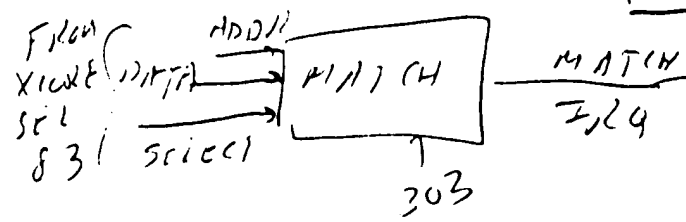


FIG. 6



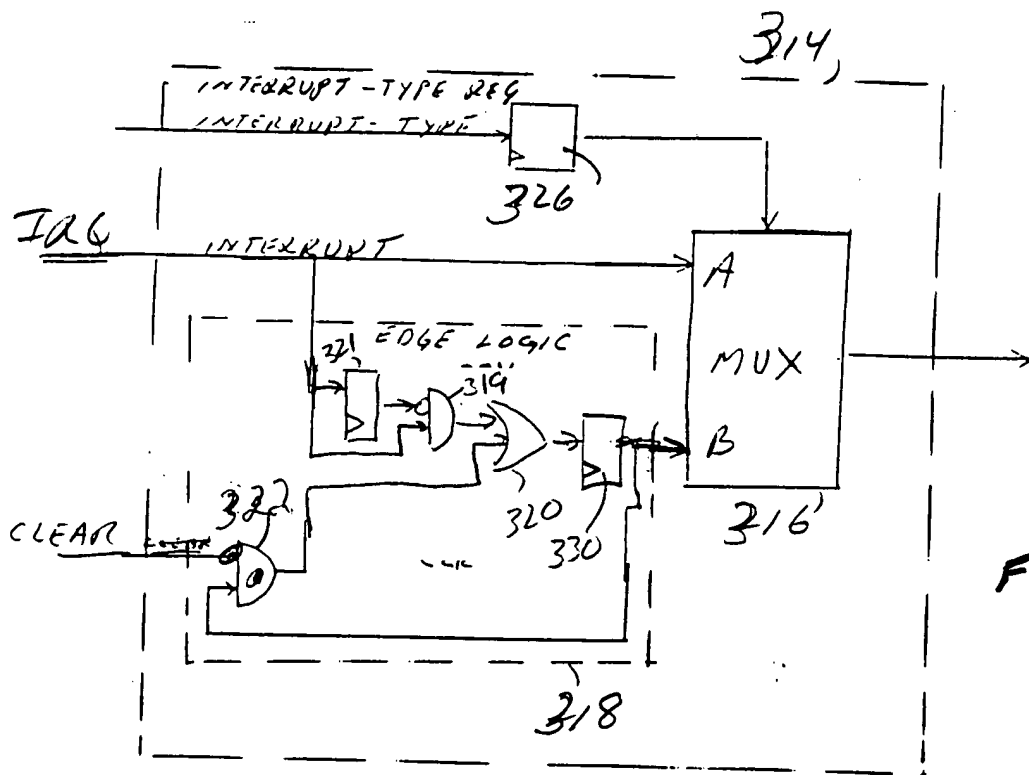


FIG 8

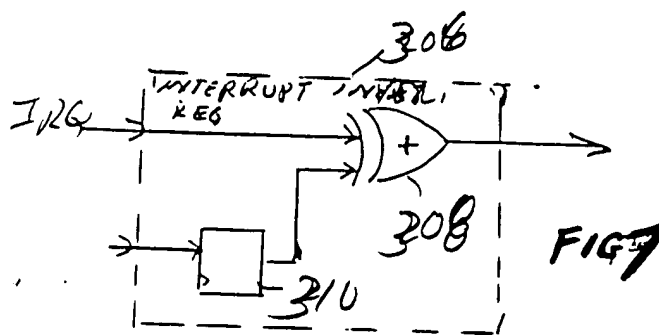


FIG 7

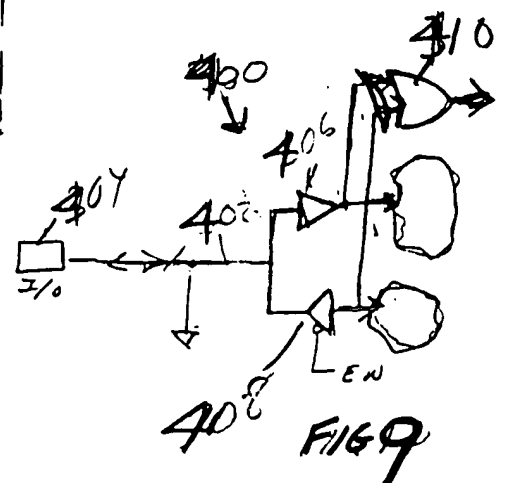


FIG 9